

(d) an interconnecting layer having electrically conductive paths thereon disposed in said cavity, each of said paths having first and second spaced apart regions thereon, said first region of each path being aligned with and contacting a said bond pad, said first region including a compliant bump probe tip having a first predetermined height above said layer and further including a standoff on said layer having a second predetermined height above said layer less than said first height; and

(e) an interconnection between said second spaced apart region of each of said paths and one of said plurality of terminals.

Amend claim 9 as follows:

9. (Amended) An interconnecting layer for use in a semiconductor package which comprises;

(a) an electrically insulating layer;

(b) electrically conductive paths on said layer, each of said paths having first and second spaced apart regions thereon, said second spaced apart region of each of said paths [being] having a compliant bump having a height greater than all other structures on said layer; and

(c) a standoff disposed on said layer and having a height above said layer and less than said bump.

Cancel claims 17 to 21 without prejudice.

Add the following claims:

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22. An apparatus adaptable for the testing of semiconductor devices comprising:

a package; and

an interconnecting medium contained within said package having electrical paths adaptable for coupling to test circuitry, wherein said interconnecting medium includes a medium surface, a plurality of standoffs affixed to said medium surface, and a plurality of probe tips affixed to said medium surface, said probe tips adaptable for making electrical contact with pads on said semiconductor device, wherein said probe tips are compliant bump probe tips.

23. The apparatus of claim 22, said package further comprising:

a package base having an upper surface adapted to receive said interconnecting medium, said medium having a medium lower surface;

a bonding layer interposed between said medium lower surface and said package base upper surface; and

a package lid having a lower surface adapted to receive said semiconductor device, wherein said package lid is positioned above said package base.

24. The apparatus of claim 23, wherein said bonding layer is comprised of an elastomeric material.

25. The apparatus of claim 23, wherein said semiconductor device is a die having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween.

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- 26. The apparatus of claim 23, wherein said semiconductor device is a wafer having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween.

27. The apparatus of claim 4, wherein said bonding layer interposed between said die and said package lid lower surface is comprised of an elastomeric material.

28. The apparatus of claim 5, wherein said bonding layer interposed between said wafer and said package lid lower surface is comprised of an elastomeric material.

29. The apparatus of claim 22, wherein the compliant bump probe tips are comprised of a solid material.

30. An apparatus adaptable for the testing of semiconductor devices comprising:

a package, wherein said package has a package lid having a lower surface adapted for receiving said semiconductor device, said semiconductor device having an upper surface, and a package base having an upper surface;

an interconnecting medium contained within said package, wherein said probe membrane has electrical paths adaptable for coupling to test circuitry, said medium including a medium surface, said medium surface having a plurality of probe tips affixed thereto, a plurality of standoffs affixed thereto, and a lower surface, wherein said probe tips are adaptable for making electrical contact with pads on said semiconductor device and are compliant bump probe tips;

a bonding layer comprising an elastomeric material interposed between said package lid lower surface and said semiconductor device upper surface; and